

APPLICATION FOR UNITED STATES LETTERS PATENT

For

**PRE-EXPOSURE OF PATTERNED PHOTORESIST FILMS TO ACHIEVE
CRITICAL DIMENSION REDUCTION DURING TEMPERATURE REFLOW**

Inventors:

Rex K. Frost

Swaminathan Sivakumar

Prepared by:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025
(408) 720-8300

"Express Mail" mailing label number: EV336587881US

Date of Deposit: December 30, 2003

I hereby state that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-14550

Christopher P. Marshall
(Typed or printed name of person mailing paper or fee)

CP Marshall
(Signature of person mailing paper or fee)

12/30/2003
(Date signed)

PRE-EXPOSURE OF PATTERNED PHOTORESIST FILMS TO ACHIEVE CRITICAL DIMENSION REDUCTION DURING TEMPERATURE REFLOW

FIELD

[0001] The present invention relates to the field of manufacturing of integrated circuits and more specifically to the reduction of patterned openings and lines in a resist layer to improve the critical dimension and reduce integrated circuit feature sizes.

BACKGROUND

[0002] The effort to build integrated circuits with more and faster semiconductor devices has resulted in a continued shrinking of the devices within an integrated circuit. This corresponds to a reduction in the size and spacing of the individual transistors and interconnections in an integrated circuit. In many applications, the switching speed and size of the switching devices are functions of the critical dimension of the MOS transistor gate and interconnections to each device. Narrower or smaller device geometries tend to produce a higher performance or faster switching transistor. For example, in circuits having MOS switching devices, a very important process step is the formation of the gate for each transistor and the formation of the interconnection paths to connect each device to form, for example, a processor integrated circuit.

[0003] The continued reduction in integrated circuit geometry sizes improves the functionalities and pricing of the integrated circuit, however, the reduction in geometry sizes continues to challenge process designers and manufacturers. The limitations of conventional lithographic techniques used to pattern transistor gates and interconnects are

quickly being realized. Accordingly, there is a continuing need for more efficient and effective fabrication processes for forming transistor gates and interconnects that are smaller and/or exhibit higher performance.

[0004] In conventional lithographic techniques, the surface of a silicon substrate wafer is coated with a light sensitive photoresist material. Once the photoresist material is formed on the surface of the silicon substrate, the wafer is aligned and the photoresist is exposed using a photo mask and a high intensity light source. The photo resist is developed, and the excess or unwanted photo resist is removed. The remaining photoresist forms a patterned mask over the surface of the silicon substrate, and is usually subjected to a baking or heating process to harden the photoresist and improve its adhesion to the substrate. The patterned photoresist mask then acts a barrier during an etch process used in the formation of semiconductor or interconnect features in an integrated circuit.

[0005] The patterned mask has characteristic qualities and limitations with regard to its ability to maintain a uniform thickness across the substrate wafer, its adhesion qualities to the substrate surface, and its ability to uniformly maintain critical dimensions transferred to it through the formation, mask exposure, development, baking, and etch processes. Design and process engineers must weigh a multitude of factors in reducing the critical dimensions in the fabrication process. Factors relating to the photoresist include thickness uniformity, the ability to hold a pattern, proximity effects during the

baking process, and etch resistance. These factors and others effectively define the resolution limit of the photoresist materials.

[0006] A critical dimension in the photoresist that is narrower than the photoresist resolution limit is generally incapable of providing an effective mask in the fabrication of a gate or interconnect. The results of using narrow dimensions beyond the resolution limit of the photoresist includes pattern collapse, bending, and pattern closures caused by proximity effects during the baking or reflow process. In addition, attempts to reduce the critical dimension by heating the resist to reflow, results in the closure of resist openings where openings are less dense or isolated in the resist mask pattern.

[0007] In particular in the example shown in Figure 1A, the structure 100, is based on a substrate 110, a dielectric layer 120, and a photoresist layer that has been subjected to the normal spin, exposure, development, and wash processes 130. The photoresist mask 130, contains an opening 150, and 151, in close proximity and an isolated opening 152. In a standard procedure following the exposure and development of a photoresist, a baking step is normally used to harden the photoresist and to improve adhesion to the surface of the substrate. Heating the resist material above the glass transition temperature of the resist material, to reflow, might be used to reduce the critical dimension of the photoresist pattern. However, holes and line patterns in the photoresist do not shrink or expand at the same rate. Heating the photoresist to reflow causes the resist to migrate at a rate that is difficult to control and some openings in the photoresist layer close. The problem also occurs when the density of openings in a patterned resist layer varies. In

areas of the photoresist mask where holes are isolated, the proximity effect and the photoresist reflow causes the isolated opening to collapse and close. This is illustrated in Figure 1B showing an isolated opening 162 that has closed while resist openings 160 and 161 do not collapse. The loss of the opening 162 is an unacceptable result.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Figure 1A illustrates a cross sectional view of a prior art patterned resist layer formed above a dielectric layer of a substrate.

[0009] Figure 1B illustrates a cross sectional view of the patterned resist of FIG 1A after reflow.

[0010] Figures 2A-2E illustrate a method to achieve critical dimension reduction in a photoresist film.

[0011] Figure 3 shows a chart of resist film contact hole diameter (DCCD) reduction versus pitch. Electron beam exposed resist reflow is compared to reflow of resist without exposure.

[0012] Figure 4 shows a chart of resist film contact hole diameter (DCCD) versus pitch. Pre-exposure of the resist material at 193nm followed by thermal reflow is compared to reflow of resist without exposure and to a standard resist process.

[0013] Figure 5 shows a table of resist film contact hole diameter (DCCD) shrinkage comparing resist exposure at 248nm followed by CD-shrink, to CD-shrink only, and to the resist with no exposure or reflow.

DETAILED DESCRIPTION

[0014] Described is a method for controlling a photoresist layer during a reflow process to develop critical dimensions beyond the resolution limit of the photoresist material, and to overcome problems associated with varying hole and line densities. After the photoresist film has been applied to a substrate, exposed, and developed, the patterned resist is exposed to electrons, photons, or ions, which modify the photoresist molecular structure. Modification of the photoresist molecular structure results in a modification of the photoresist reflow characteristics which results in improved control over the rate that the resist collapses or flows into openings or lines in the photoresist pattern.

[0015] In one embodiment, as show in Figure 2A, an underlying substrate 210 contains formed switching devices, with an inter level dielectric layer 220 formed above the substrate in preparation for forming conductive interconnects. However, in other embodiments, the underlying substrate may contain partially formed switching devices with the intent of forming features to the partially formed devices. After a photoresist layer 228, is formed or spun above a substrate 220, in Figure 2B, the photoresist layer is exposed, developed, and further processed to remove any unwanted resist or contaminants to develop a patterned resist mask 230. In one embodiment, a post development soft bake process, executed below the resist glass transition temperature, is not employed. In another embodiment, the patterned resist may be subject to a post development soft bake process as a dehydration step, executed below the glass transition temperature for the particular resist material being used.

[0016] In one embodiment, a 193nm sensitive resist material, is used. However, a variety of standard resist materials may be used, for example, any chemically amplified or non-chemically amplified resist material, such as I-line, ArF, EUV, or resists sensitive to 248nm, 193nm, or 157nm light sources. Typical 193nm resists include acrylate, methacrylate and other hybrids. Also, the geometry size does not particularly matter, and it is possible to implement the process using 248nm geometries or smaller. As shown in Figure 2B, the patterned photoresist 230, with openings 240, 241, and 242 would have acted as a mask to expose the underlying substrate 220 to an etch process. However, smaller openings are desired.

[0017] Next, as shown in Figure 2C, the patterned photoresist layer is exposed 250, either to an electron beam, a light source, an ion source, or a combination of sources. In one embodiment, using a 193nm sensitive methacrylate film, an electron beam flood exposure is performed, using an ElectronVision ECA3C, and implemented at 1.5K to 2.5K electron volts, with a density of 2,000 micro-Coulombs per square centimeter, at a normal angle of exposure, is performed for between 20 to 40 seconds. A variety of resist materials may be used, and the exposure parameters may vary outside of the above ranges, depending on the individual and specific photoresist that is being used. Variations in the parameters for each resist film is generally governed by the absorption cross-section and required de-protection energies of the individual resist material being used. The general formula or parameters may be easily changed to vary the exposure of a particular photoresist to optimize each resist material's characteristics.

[0018] The electron beam exposure of the photoresist results in a polymer modification, a de-protection, or decomposition modification of the photoresist material. The electron beam may cleave the backbone of the polymer or create a cross-linking mechanism that results in a modification to the molecular weight and/or the glass transition temperature of the resist. Typical methacrylate resists normally have Tg of approximately 150-170C. An electron beam exposure will normally reduce this value to approximately 120-140C. Without cleaving the backbone of the resist material, the molecular weight is expected to change by approximately 10% to 30%. However, depending on the photoresist material used and the electron beam exposure parameters, the invention is not limited to these particular modifications to the molecular structure of the photoresist material.

[0019] Alternately, a patterned photoresist film may be exposed to photons or ions, resulting in similar beneficial changes to the resist film material. In one embodiment, the photoresist material is exposed to a light source such as a flash lamp, at a variety of frequencies, for example at wavelengths of 193nm or 248nm. Exposure conditions are normally kept below the solvation-switch deprotection threshold (E0), and will generally be governed by the relative cross-section of the resist film.

[0020] In one embodiment using a 193nm sensitive methacrylate film, a flood exposure of approximately 4 to 6 mJoules per square centimeter for approximately 30 seconds will yield a change in the resist characteristics. In another embodiment, for a

248nm sensitive film, an exposure to a light source at approximately 10mJoules per square centimeter for approximately 30 seconds will modify the resist characteristics. Exposing a variety of resist types to a photon source at densities similar to the embodiments described above will alter the characteristics of a resist film. Although the above embodiments are for 193nm and 248nm sensitive resist films with exposure to a corresponding light source, a variety of wavelengths and light sources may be used.

[0021] Next, a patterned resist exposure is followed by a thermal reflow by heating the photoresist to or beyond its post exposure glass transition temperature. Figure 2D illustrates a substrate 210, an inter-level dielectric layer 220, and a patterned photoresist film 231, after having been exposed to electrons, photons, or ions, and subsequently heated to or beyond the glass transition temperature. A post-exposure resist will provide improved control and more uniform opening sizes without closure or collapse, from the proximity effect during a reflow, in comparison to the same resist material that was not exposed. The openings 260 and 261 have been reduced, and isolated opening 262 will experience a similar reduction in opening size without collapse, in comparison to the pre-exposure resist patterns shown in Figure 2B. The exposure, having modified the resist material to create a more uniform shrinkage characteristic, provides the ability to control the shrinkage rate during a subsequent resist reflow process to reduce the opening or line of a resist pattern.

[0022] In one embodiment, the exposure of a photoresist material to an electron beam subsequently followed by a thermal reflow process modifies the observed reflow

magnitude response of the photoresist by approximately 10 to 15 percent. A photoresist exposed to an electron beam using the above method, compared to photoresist that has not been exposed, will exhibit a more uniform shrinkage rate of openings in the photoresist relative to a varying pitch or distance between patterned resist openings or lines. In one embodiment, after exposure to an electron beam, the photoresist layer is then heated to or beyond the post exposure glass transition temperature of the photoresist material to between 125 to 180 degrees Centigrade for 60 to 90 seconds. This operating range may be used for various resist materials. However, the bake requirements or ranges will be different for each resist material depending on the glass transition temperature (T_g) of the resist polymer. In general, pure acrylate resists are expected to have a glass transition temperature (T_g) appropriate for thermal reflow, but typically have a less competitive lithographic resolution. Resists with more methacrylate character typically have better lithographic performance but have a relatively high T_g. In one embodiment, a single resist was used, but final optimized solutions would normally employ different resins. It is not expected that one solution would necessarily provide a lower fundamental critical dimension (CD) limit than another.

[0023] Modifying the resist response at or above the glass transition temperature provides better control over the reduction rate of the photoresist layer openings and provides a reduction of the critical dimension to below the resolution of a lithographic tool set or below the photoresist fundamental resolution. The modification of the photoresist molecular structure also produces a change in the glass transition temperature

(T_g). A modification to the glass transition temperature will allow matching a resist's characteristics to a desired heating process.

[0024] Using the above exposure method, a decrease in a critical dimension in a patterned resist layer in preparation for a subsequent etch process may be achieved. A variety of etch techniques are applicable, such as a wet or gaseous chemical or isotropic etch, or a dry plasma, reactive ion, or anisotropic etch to either develop device interconnections or to develop features of a switching device such as an MOS transistor. In Figure 2E, the etch process creates openings 263, 264, and 265, in dielectric layer 221 that are smaller than the resist openings produced by a lithographic tool set, or the fundamental resolution of the photoresist, as illustrated in Figure 2B as 240, 241, and 242. The etch process may be used to form the openings for conductive interconnections between electronic or digital switching devices or to form the feature of an electronic or digital switching device.

[0025] In Figure 3, an “electron beam exposure/cure plus reflow” is compared to a “resist reflow without electron beam cure.” The measurements are compared in chart format as “resist film contact hole diameter reduction DCCD (develop check critical dimension) versus pitch.” The chart indicates that a beneficial critical dimension reduction is not achieved at tighter pitches without the electron beam exposure step. The “electron-beam cure followed by reflow” curve is relatively flat from approximately a 300nm pitch to 900 nm pitch in comparison to the same resist material that has not been

subjected to the electron beam exposure. In this embodiment, the exposed resist pattern exhibits a controllable 10 to 15 percent reduction in the critical dimension. In addition, for the “electron-beam cure followed by reflow” resist, the shrinkage with respect to pitch is fairly constant, indicating a reduction in the proximity effect for the resist material that has been exposed. The curves in Figure 3 indicate that an electron beam exposure of photoresist material will mitigate pitch related resist problems when the resist film reflows and shrinkage occurs.

[0026] In Figure 4, pre-exposure to a 193nm light source followed by thermal reflow is compared to reflow only and a standard lithographic process with no treatment. Figure 4 compares: 1) a lithography patterned resist, 2) the same resist material heated to or beyond its glass transition temperature to reflow, and 3) the same resist material exposed to a 193nm light source followed by thermal reflow. For the resist subjected to a standard lithography process, the response in comparison to pitch is linear from approximately 400nm to 1,000nm. In comparison, the resist material without exposure but with reflow exhibits a rapid and non-uniform shrink rate, causing closures due to the proximity effect of the resist material. The reflow curve for the resist that has been exposed to the 193nm light source provides improved control and uniformity in comparison to the resist that was not exposed. The data curves indicate a beneficial critical dimension reduction is not achieved at tight pitch without exposure.

[0027] The above exposure parameters may be varied to modify changes to the resist characteristics during reflow. In Figure 4, the reflow curve lies above both the standard

resist lithography process and the non-exposed resist with reflow curve. However, an exposed resist material's curve may be adjusted above or below the lithography and reflow only resist curves.

[0028] Figure 5 shows similar data for a photoresist material exposed to a 248nm light source. The data indicates that the thermal processing is constant between the resist materials that have been subjected to reflow, with a greater available control of shrinkage for the resist material that has been exposed.

[0029] The patterned resist may also be exposed to ions by accelerating charged atoms to expose and/or cleave the molecular backbone structure of the resist material. In this embodiment of using an ion source to expose the resist, the same result of modifying the reflow characteristics and the glass transition temperature of various photoresist materials will also be achieved. The process of exposing the photoresist layer to electrons, photons, or ions may be used to modify the thermal response or reflow characteristics and to modify the resist glass transition temperature, to match the post exposure resist characteristics to a desired process. For example, matching the resist reflow and glass transition characteristics to preferred heating and temperature profiles.

[0030] It can be seen in Figure 3, 4, and 5 that the reflow curve of a resist material that has been pre-exposed to an electron beam or a photon source, may yield more control over a subsequent thermal reflow process. The photoresist materials used in the described embodiments have been shown to provide a variety of response changes and a

variety of changes to the glass transition temperatures related to a variety of photoresist materials when compared to a variety of exposure processes. Also, a variety of embodiments of the invention provide the ability to modulate and control the shrinkage characteristics of the resist material during reflow.

[0031] In the described method above, a photoresist material has been shown to provide a variety of reflow responses related to an exposure process. The process of exposing a patterned photoresist layer to an electron beam, photon, or ion source may be used to modify the thermal response or reflow characteristics of a resist material to control the rate in which openings or lines shrink, ultimately controlling at least one critical dimension in a semiconductor or integrated circuit manufacturing process.

[0032] Alternate embodiments of the invention may provide the ability to modulate and control the shrinkage characteristics of a variety of resist materials. Although the embodiments described may represent specific resist materials subjected to specific exposure parameters, using alternate resists, other solvents or combination of solvents, and alternate exposure parameters will provide similar beneficial modifications to the resist reflow response. In addition, a particular resist material may be matched to a desired thermal cycle to keep the resist layer below a degradation point.

[0033] While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not

restricted to the specific constructions and arrangements shown and described since modifications may occur to those ordinarily skilled in the art. In other instances well-known semiconductor fabrication processes, techniques, materials, equipment, etc., have not been set forth in particular detail in order to not unnecessarily obscure the present invention.